A Novel Commutation Strategy to Suppress the Common Mode Voltage for the Matrix Converter

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***Abstract*—The double line-to-line voltage synthesis of matrix converter is based on the instantaneous value of the input line-to-line voltage. And the obvious advantage of this modulation strategy to automatically suppress the imbalance of the input voltage makes it excellent in the modulation strategy of the matrix converter. Considering the EMI issue in driver system based on matrix converter, common mode voltage is of great importance. Reducing the common voltage actively could be achieved by designing the proper modulation strategy a new modulation strategy with reduced common voltage in the context of double line-to-line voltage synthesis is proposed in this paper. It is based on the idea without employing zero vectors instead of the vectors which are opposite to the active vectors in space vector modulation. The modulation strategy is verified by the simulations finally.**

Keywords- Double line-to-line voltage synthesis, common mode voltage, commutation strategy, Matrix Converter

I. INTRODUCTION

Matrix converter is a new type topology with several advantages, which includes the bidirectional energy flow, sine waveform of the input current, controllable power factor and small but compact structure. Since the topology has been proposed in 1976, several modulation strategies have been proposed. They are switching functions method[1], space vector modulation [2-3] (SVM) and the double line-to-line voltage synthesis [4-9] (DLLVS). Since the space vector modulation has been the defacto standard method. There are less literatures focusing on the double line-to-line voltage synthesis. With the method proposed by the Japanese scholar A.ishiguro in[4], the basic advantages are the modulation strategy can automatically suppress the fluctuation on the load, realize the unity power factor and the maximum line voltage transfer ratio. And the concept, the source key is proposed in [5] to simplify the realization. [7] and [8] have studied the common mode voltage under the modulation strategy, and the commutation strategies are given. Based on the analyses of the zero vectors voltages, a novel modulation is proposed in this paper and the proposed scheme is verified by the simulation result.

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II. PRINCIPLES OF THE COMMUTATION STRATEGY

A. Topology of the matrix converter

The typical topology of the AC/AC matrix converter (MC) is shown in Fig.1. and the switches S_{ij} ($i \in \{a,b,c\}$, $j \in \{A,B,C\}$)is the bidirectional switch.

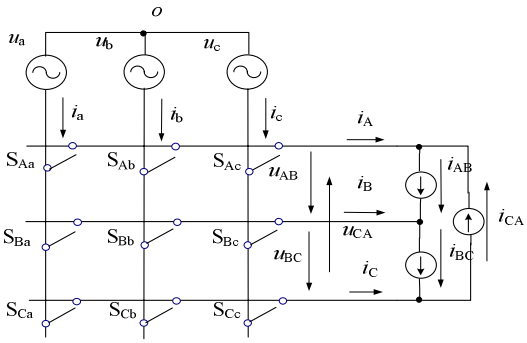

Fig. 1 The simplified direct topology of matrix converter

Suppose the three-phase input voltages are

$$\begin{cases} u_a = U_{im}\cos(q) \\ u_b = U_{im}\cos(q - 2p/3) \\ u_c = U_{im}\cos(q + 2p/3) \end{cases} \quad (1)$$

And the desired three-phase output voltages are

$$\begin{cases} u^*_{AB} = U_{om}\cos(\beta) \\ u^*_{BC} = U_{om}\cos(\beta - 2\pi/3) \\ u^*_{CA} = U_{om}\cos(\beta + 2\pi/3) \end{cases} \quad (2)$$

B. The principles of the double lien-to-line synthesis

The duty cycle coefficients of the DLLVS are calculated to control the 9 bidirectional switches, and the desired output line -to-line voltage is chose properly from the double input line-to-line voltage. Suppose the input voltage is in the Sector 1 in Fig. 3(a) (namely, the Sector *I* in Fig. 2(a)). And the output voltage is in the Sector 1 in the Fig. 1 (namely, the Sector *I* in Fig. 2(b)). Based on the principle, the equation 10 is derived.

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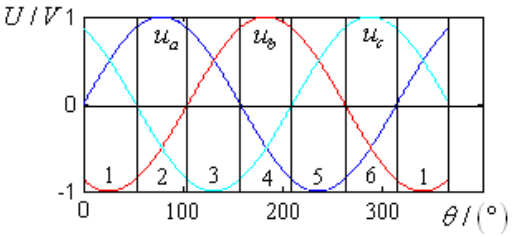
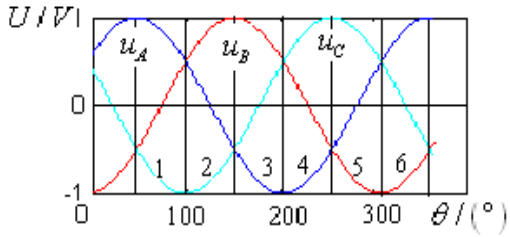


(a) The sector partition of the input phase voltage



(b) The sector partition of the output phase voltage

Fig. 2 sectors of the phase voltage

$$\begin{cases} u_{AB}^{*} = u_{ab}d_{11}^{'} + u_{ac}d_{12}^{'} \\ u_{AC}^{*} = u_{ab}d_{21}^{'} + u_{ac}d_{22}^{'} \end{cases} \quad (3)$$

Where, the duty cycles $d_{11}^{'}, d_{12}^{'}, d_{21}^{'}, d_{22}^{'}$ must meet the constraint equations (4)。

$$\begin{cases} 0 \le d_{11}^{'}, d_{12}^{'} \le 1, 0 \le d_{21}^{'}, d_{22}^{'} \le 1 \\ 0 \le d_{11}^{'} + d_{12}^{'} \le 1, 0 \le d_{21}^{'} + d_{22}^{'} \le 1 \end{cases} \quad (4)$$

According to the calculation method mentioned in [4], the equations 5 below can be derived

$$\begin{cases} d_{11}^{'} = -k \cdot u_{AB}^{*} \cdot u_b \\ d_{12}^{'} = -k \cdot u_{AB}^{*} \cdot u_c \\ d_{21}^{'} = -k \cdot u_{AC}^{*} \cdot u_b \\ d_{22}^{'} = -k \cdot u_{AC}^{*} \cdot u_c \end{cases} \quad (5)$$

Where, k can be expressed in (6)

$$k = \frac{3}{u_{ab}^2 + u_{ca}^2 + u_{bc}^2} \quad (6)$$

When the input three-phase voltages are symmetric the equation 6 can be simplified

$$k = \frac{1}{1.5U_{im}^2} \quad (7)$$

The left time during each sample period can be supplemented with zero-voltage components $d_{10}^{'}, d_{20}^{'}$

$$\begin{cases} d_{10}^{'} = 1 - d_{11}^{'} - d_{12}^{'} \\ d_{20}^{'} = 1 - d_{21}^{'} - d_{22}^{'} \end{cases} \quad (8)$$

The corresponding line-to-line voltage of $d_{10}^{'}, d_{20}^{'}$ are $u_{aa} = 0$.

C. The common mode suppression strategy

The expression of the common mode voltage is $u_{com} = (u_A + u_B + u_C)/3$, which represents the average value of the instantaneous voltages between the output terminal and the reference point (usu. the ground). The common mode voltage will bring great harm. As for lessening the common mode voltage, there exist two ways. One is to equip the system with the auxiliary devices while the other is to change the modulation strategy. The matrix converter adopts more switches than the inverter and has lots of freedom degree as a result. So it is easy to implement the novel modulation strategies to lesson the common mode voltage.

There are 21 switch combinations in the MC ,which can be divided into two parts of the effective switch states and the zero switch states. Consider the input current and the line-to-line voltage in the Sector 1 as an example, within the effective switch states, the common mode voltage set is $u_{com} \in \{u_{bc}/3, u_{ac}/3, u_{cb}/3, u_{ab}/3, u_{ca}/3, u_{ba}/3\}$, and the range of the u_{com} is derived, $|u_{com}| \le \sqrt{3}/3 U_{im}$, while the corresponding common mode voltage set is $u_{com} \in \{u_a, u_b, u_c\}$ within zero switch states. As the easiest implementation, the zero vector, of which the input instantaneous voltage is the least, is chose as the common mode voltage, namely, $u_{com} = \min(u_a, u_b, u_c)$ to suppress the common mode voltage.

Inspired by the space vectors to utilize the adverse vectors to suppress the common mode voltage, a similar modulation strategy is proposed here. But the implementation is quite different. While in the space vector modulation, there exists two opposite effective vectors, the common mode voltage needs to be suppressed with the three effective vectors due to the different topology. More precisely speaking, the combined effect of the three effective vectors with the mutual angle difference 120° will be a zero vector, which means no common mode voltage at all.

According to the source keys proposed in [4], the common mode voltage suppression is needed to be conducted in each source key segment. Take the source key segment IX for example, the common mode voltage suppression diagram is shown below, while both the line-to-line voltage(generated by the adverse switch combination) and the common mode voltage are considered here.

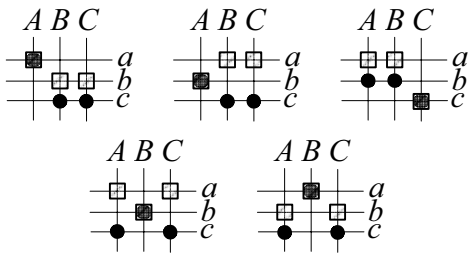


Fig.3 The common mode voltage suppression for the source key segment *IX*

- The calculation of the duty cycle

The common mode voltage, which can be suppressed only within the zero voltage component, and the duty cycle for the three effective vectors is easy to calculate and the expression is given below. Since the relationship between the each duty cycle is not constant, so the switching sequence of the duty cycle may sound very difficult here. For the sake of the easy implementation and verification, we adopts the easiest time arrangement, which divides the duty cycle for the zero voltage component into ten parts, namely, $d_i=d_0/10$, (d_i denotes one of the ten switches, $d_0$denotes the zero voltage component)

- The switching sequence of the duty cycle

The switching states for the source key segment IX can be depicted in the figure below with 244, for example, denotes the S1~S9=010 100 100, the solid line represents the switch change only once between the neighboring switching states and the dash line represents twice of the switch change.

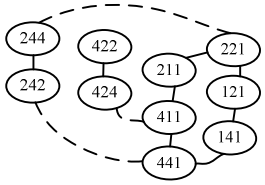
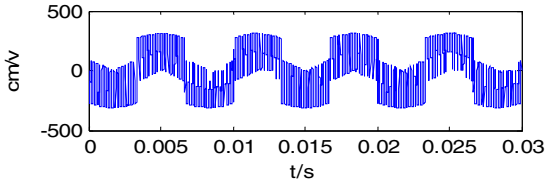


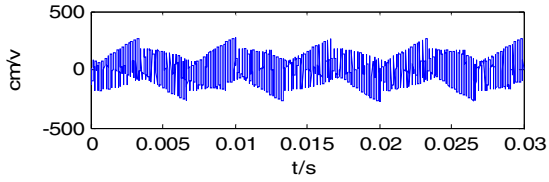
Fig. 4 the 10 switch states for the zero voltage component

III. SOFTWARE VERIFICATION

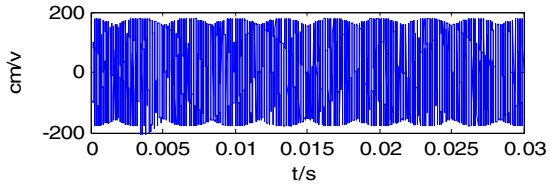
With the 10 switch states and the duty cycle, we can easily implement the proposed commutation strategy and the proposed schemes are verified by the Matlab/Simulink with the simulation conditions, the amplitude of the input phase voltage $U_i = 220\sqrt{2}\,V$, the input frequency is $f_i=50Hz$,the output frequency is $f_o=50Hz$, and the voltage transfer ratio is 0.5, the switching frequency is *5kHz* and the load is $Z=1+j0.3$.



a) the common mode voltage of the original DLLVS



b) the common mode voltage of choosing the least phase voltage



c) the common mode voltage of choosing a pair of adverse vectors

Fig. 5 the comparison about the common mode voltage

The common mode voltage output of the conventional DLLVS is shown in the Fig. 5(a), while Fig. 5(b) shows the result of choosing the least phase voltage as a zero voltage. And the Fig. 5(c) is the simulation result of the proposed strategy. After the comparisons between them, the conclusion can be derived that the utilization of the three vectors, of which the mutual angle difference is 120° can obviously suppress the common mode voltage. Although the amplitude is similar to the result of choosing the least phase voltage as a zero voltage, the voltage waveform is rather smooth. That means, the electromagnetic interference(EMI) brought with dV/dt will be reduced much. As a result, the application field of this DLLVS will be broadened.

IV. CONCLUSION

Based on the analyses of the double line-to-line voltage synthesis modulation strategy and the switch states, a novel strategy is proposed with choosing the three phase voltage, of which the mutual difference is 120° to generate within the zero voltage component in each sample period. And the proposed strategy is verified by the simulation. What's more, the more smoothness and lower amplitude advantages make this strategy more promising in the future adjustable speed drive(ASD) field.

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